CLAIMS

Having thus described the invention, what is claimed as new and desirable to be secured by Letters Patent is as follows:

1. A method for fabricating a Silicon Based Package (SBP) comprising the steps of:

starting with a wafer composed of silicon and having a first surface and an initial reverse surface which are substantially planar as the base for the SBP;

forming a first interconnection structure over the first surface;

then forming a protective overcoat layer over the interconnection structure;

forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure;

thinning the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP;

forming Vertical Sidewall Through Via (VSTV) holes which extend through the UTSW with the VSTV holes having bases and substantially vertical sidewalls; and

forming metallization in the VSTV holes with the metallization extending through the UTSW.

2. The method of claim 1 including the step of bonding the metallization in the VSTV holes to pads of a carrier.

3. The method of claim 1 including the step of forming metal capture structures over the first surface prior to thinning the wafer.

4. The method of claim 1 including the steps of:

initially forming metal capture structures over the first surface;

then forming the interconnection structure over the first surface and the metal capture structures;

then forming the protective overcoat layer;

then forming the temporary bond of the wafer holder to the protective overcoat layer; and

then thinning the wafer on the initial reverse surface, thereby forming the UTSW, with a thinned reverse surface.

5. The method of claim 1 including the steps of:

initially forming metal capture structures over the first surface;

then forming the interconnection structure over the first surface and the metal capture pads;

then forming the protective overcoat layer;

then forming the temporary bond of the wafer holder to the protective overcoat layer;

then thinning the wafer on the initial reverse surface, thereby forming the UTSW, with a thinned reverse surface; and

then forming the VSTV holes through the UTSW with the sidewalls of the VSTV holes reaching down to form VSTV bases on the metal capture structures.

6. The method of claim 1 including the steps of:

initially forming metal capture structures over the first surface;

then forming the interconnection structure over the first surface and the metal capture structures;

then forming the protective overcoat layer;

then forming the temporary bond of the wafer holder to the protective overcoat layer;

then thinning the wafer, thereby forming the UTSW, with a thinned reverse surface;

then forming the VSTV holes through the UTSW with the sidewalls of the VSTV holes reaching down to form VSTV bases on the metal capture structures;

then forming a dielectric layer over the surface of the wafer leaving the bottoms of the VSTV holes clear over the metal capture structures; and

then forming metal pads in the VSTV holes in contact with the metal capture structures.

7. The method of claim 1 including the steps of:

initially forming metal capture structures over the first surface;

then forming the interconnection structure over the first surface and the metal capture structures;

then forming the protective overcoat layer;

then forming the temporary bond of the wafer holder to the protective overcoat layer;

then thinning the initial reverse surface of the wafer, thereby forming the UTSW, with a thinned reverse surface;

then forming the VSTV holes through the thinned reverse surface of the UTSW with the sidewalls of the VSTV holes reaching down to form VSTV bases on the metal capture structures;

then forming a dielectric layer over the surface of the UTSW including the thinned reverse surface, leaving the bottoms of the VSTV holes clear with the metal capture structures exposed;

then depositing metal pads into the VSTV holes in contact with the metal capture structures; and

then forming metal joining structures on the metal pads.

8. The method of claim 1 including forming the VSTV holes in the thinned reverse surface after thinning the wafer.

9. The method of claim 1 including the steps of:

thinning the initial reverse surface of the wafer, thereby forming the UTSW, with a thinned reverse surface;

forming the VSTV holes in the thinned reverse surface after thinning the wafer; and

then forming a dielectric layer covering the VSTV holes.

10. The method of claim 1 including the steps of:

initially forming metal capture structures over the first surface;

thinning the initial reverse surface of the wafer, thereby forming the UTSW with a thinned reverse surface;

forming the VSTV holes in the thinned reverse surface after thinning the wafer;

then forming a dielectric layer over the surface of the wafer including the VSTV holes; and

then etching the dielectric layer to expose the surface of the metal capture structures at the bases of the VSTV holes.

11. The method of claim 1 including the steps of:

initially forming metal capture structures over the first surface;

then thinning the initial reverse surface of the wafer by a method selected from chemical mechanical planarization and plasma processing, thereby forming the UTSW, with a thinned reverse surface;

forming the VSTV holes in the thinned reverse surface after thinning the wafer;

then forming the VSTV holes through the thinned reverse surface of the UTSW with the sidewalls of the VSTV holes reaching down to form VSTV bases on the metal capture structures;

then forming a dielectric layer over the thinned reverse surface of the wafer including the VSTV holes;

then etching the dielectric layer to expose the surface of the metal capture structures at the bases of the VSTV holes;

then depositing metal pads into the VSTV holes in contact with the metal capture structures;

then forming metal connectors on the metal pads.

12. The method of claim 1 including the steps of:

initially forming metal capture structures over the first surface;

thinning the initial reverse surface of the wafer by subtractive processing, thereby forming the UTSW, with a thinned reverse surface;

forming the VSTV holes in the thinned reverse surface after thinning the wafer to provide exposed metal capture structures;

then forming a dielectric layer over the thinned reverse surface of the UTSW and the sidewalls and bases of the VSTV holes and the exposed metal capture structures;

then removing the dielectric layer from horizontal surfaces including the exposed metal capture structures;

then forming metal pads comprising a metal layer on the exposed metal capture structures and sidewalls of the VSTV holes;

then forming metal connectors on the metal pads; and

then joining the metal connectors to a carrier body.

13. The method of claim 12 including the steps of:

forming a dielectric hard mask with a pattern of VSTV openings therethrough over the thinned reverse surface of the wafer; and

forming the VSTV holes through the thinned reverse surface through the dielectric VSTV hard mask layer to form VSTV holes exposing in the after thinning the wafer to provide exposed metal capture structures.

14. A method for fabricating a Silicon Based Package (SBP) comprising the steps of:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are substantially planar;

then forming metal capture structures over the first surface;

then forming a temporary bond between the wafer and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed;

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP with a thinned reverse surface of the wafer;

then forming Vertical Sidewall Through Via (VSTV) holes with sidewall surfaces and bases which extend from the thinned reverse surface through the wafer with each VSTV hole extending to a surface of the metal capture structures;

then forming a dielectric layer covering the first surface of the silicon wafer including the sidewall surfaces and bases of the VSTV holes;

then etching the dielectric layer to expose the surface of the metal capture structures at the bases of the VSTV holes;

then forming metal pads in the VSTV holes on exposed surfaces thereof with proximal ends being located at the thinned reverse surface and distal ends of the metal pads being in contact with the metal capture structures at the bases of the VSTV holes; and

then forming solder connectors on the metal pads in the VSTV holes.

15. The method of claim 14 including the steps of:

forming a patterned dielectric hard mask with a pattern of VSTV openings therethrough over the thinned reverse surface of the wafer; and

forming the VSTV holes by etching through the pattern of VSTV openings through the patterned dielectric VSTV hard mask layer and the thinned reverse surface to form VSTV holes, thereby exposing the surface of the metal capture structures.

16. The method of claim 14 including the steps of:

forming the temporary bond with polyimide; and

releasing the temporary bond by laser ablation.

17. The method of claim 16 including the steps of:

forming a patterned dielectric hard mask with a pattern of VSTV openings therethrough over the thinned reverse surface of the wafer; and

forming the VSTV holes by etching through the pattern of VSTV openings through the patterned dielectric VSTV hard mask layer and the thinned reverse surface to form VSTV holes, thereby exposing the surface of the metal capture structures; and

then releasing the temporary bond by laser ablation.

18. The method of claim 14 including the step of bonding the solder ball connectors on the metal pads in the VSTV hole to pads of a carrier.

19. The method of claim 14 including the step performed prior to thinning of the wafer of burying metal capture pads in a dielectric layer and forming at least one small diameter capture via between each metal capture pad and the first surface of the wafer.

20. A silicon based package (SBP) comprising:

an ultra thin silicon wafer (UTSW) composed of silicon and having a first surface and a reverse surface;

metal capture structures formed on the first surface;

an interconnection structure formed over the first surface and the metal capture;

VSTV holes formed in the SBP which extend from the reverse surface through the UTSW to the metal capture structure; and

metal pads formed in the VSTV holes which extend through the UTSW into contact with the metal capture structure.